WHAT IS CLAIMED IS:

1. A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer generates equalized data; and

a clock and data recovery circuit coupled to the decision feedback equalizer, wherein the clock and data recovery circuit generates an extracted clock signal from the equalized data and wherein the decision feedback equalizer includes a retimer that generates recovered equalized data from the equalized data in response to the extracted clock signal.

2. The communications system of claim 1 wherein the decision feedback equalizer comprises a summer that generates a combined signal by combining an equalized feedback signal with the received data to reduce the channel related distortion.

3. The communications system of claim 2 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer generates the equalized data by converting the combined signal into a binary signal and wherein the clock and data recovery circuit generates the extracted clock signal from the binary signal.

4. The communications system of claim 3 wherein the retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit and wherein the flip flop generates recovered equalized data from the binary signal in response to the extracted clock signal.

5. The communications system of claim 3 wherein the clock and data recovery circuit comprises a frequency

acquisition loop and a phase lock loop, wherein the frequency acquisition loop adjusts frequency of the extracted clock signal to maintain a fixed relationship between frequency of the binary signal and the frequency of the extracted clock signal and wherein the phase lock loop adjusts phase of the extracted clock signal to maintain a fixed relationship between phase of the binary signal and the phase of the extracted clock signal.

6. The communications system of claim 5 wherein the clock and data recovery circuit further comprises a frequency lock detector for determining when the frequency of the extracted clock signal is fixed relative to the frequency of the binary signal.

7. The communications system of claim 6 wherein the decision feedback equalizer further comprises a multiplier coupled to the retimer and wherein the multiplier applies an equalization coefficient to the recovered equalized data to generate the equalized feedback signal.

8. The communications system of claim 7 wherein the multiplier applies a predetermined equalization coefficient upon start up.

9. A communication system comprising:

a transmitter transmitting an information signal over a communication media; and

a receiver coupled to the communication media for receiving the transmitted information signal, wherein the receiver comprises:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the

decision feedback equalizer generates equalized data, and

a clock and data recovery circuit coupled to the decision feedback equalizer, wherein the clock and data recovery circuit generates an extracted clock signal from the equalized data and wherein the decision feedback equalizer includes a retimer that generates recovered equalized data from the equalized data in response to the extracted clock signal.

10. The communications system of claim 9 wherein the decision feedback equalizer comprises a summer that generates a combined signal by combining an equalized feedback signal with the received data to reduce the channel related distortion.

11. The communications system of claim 10 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer generates the equalized data by converting the combined signal into a binary signal and wherein the clock and data recovery circuit generates the extracted clock signal from the binary signal.

12. The communications system of claim 11 wherein the retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit and wherein the flip flop generates recovered equalized data from the binary signal in response to the extracted clock signal.

13. The communications system of claim 11 wherein the clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop, wherein the frequency acquisition loop adjusts frequency of the extracted clock signal to maintain a fixed relationship between frequency of

the binary signal and the frequency of the extracted clock signal and wherein the phase lock loop adjusts phase of the extracted clock signal to maintain a fixed relationship between phase of the binary signal and the phase of the extracted clock signal.

14. The communications system of claim 13 wherein the clock and data recovery circuit further comprises a frequency lock detector for determining when the frequency of the extracted clock signal is fixed relative to the frequency of the binary signal.

15. The communications system of claim 14 wherein the equalizer further comprises a multiplier coupled to the retimer and wherein the equalizer applies an equalization coefficient to the recovered equalized data to generate the equalized feedback signal.

16. The communications system of claim 15 wherein the multiplier applies a predetermined equalization coefficient upon start up.

17. A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, the decision feedback equalizer comprising:

a summer that combines an equalized feedback signal with the received data,

a slicer coupled to the summer, wherein the slicer converts the combined signal to a binary signal,

a retimer coupled to the slicer, wherein the retimer generates recovered equalized data from the binary signal in response to an extracted clock signal, and

a multiplier coupled to the retimer, wherein the multiplier applies an equalization coefficient to the recovered equalized data to generate the equalized feedback signal, and

a clock and data recovery circuit coupled to the slicer, wherein the clock and data recovery circuit generates the extracted clock signal from the binary signal.

18. The communications system of claim 17 wherein the clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop, wherein the frequency acquisition loop adjusts frequency of the extracted clock signal to maintain a fixed relationship between frequency of the binary signal and the frequency of the extracted clock signal and wherein the phase lock loop adjusts phase of the extracted clock signal to maintain a fixed relationship between phase of the binary signal and the phase of the extracted clock signal.

19. The communications system of claim 18 wherein the clock and data recovery circuit further comprises a frequency lock detector for determining when the frequency of the extracted clock signal is fixed relative to the frequency of the binary signal.

20. The communications system of claim 19 wherein the multiplier applies a predetermined equalization coefficient upon start up.

21. A method of reducing channel related distortion in received data comprising:

providing received data to a decision feedback equalizer;

generating, by the decision feedback equalizer, a binary

signal according to the received data;

extracting a clock signal from the binary signal; and

retiming the binary signal according to the clock signal.

22. The method of claim 21 further comprising:

maintaining a fixed frequency relationship between the binary signal and the extracted clock signal by adjusting the frequency of the extracted clock signal; and

maintaining a fixed phase relationship between the binary signal and the extracted clock signal by adjusting the phase of the extracted clock signal.

23. The method of claim 22 wherein the fixed phase relationship is maintained after determining that the frequency of the extracted clock signal is fixed relative to the frequency of the binary signal.

24. The method of claim 21 further comprising applying at least one predetermined equalization coefficient to the decision feedback equalizer upon startup.

25. The method of claim 21 further comprising modifying at least one equalization coefficient to synchronize frequencies of the extracted clock signal and the binary signal.

26. The method of claim 25 further comprising adjusting at least one equalization coefficient to reduce inter-symbol interference after synchronizing the frequencies of the extracted clock signal and the binary signal.